(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 July 2003 (03.07.2003)

PCT

(10) International Publication Number
WO 03/055086 A1

(51) International Patent Classification[7]: H04B 1/12

(21) International Application Number: PCT/SG01/00256

(22) International Filing Date: 20 December 2001 (20.12.2001)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **NATIONAL UNIVERSITY OF SINGAPORE** [SG/SG]; 10 Kent Ridge Crescent, Singapore 119260 (SG).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **MARATH, Ashok, Kumar** [IN/SG]; Apartment Block 730, Yishun Street 71, #09-43, Singapore 760730 (SG). **SYED, Naveen, Altaf, Ahmed** [IN/SG]; Block 46, Telok Blangah Drive, #03-73, Singapore 100046 (SG).

(74) Agent: **ELLA CHEONG MIRANDAH & SPRUSONS PTE LTD**; Robinson Road Post Office, P.O. Box 1531, Singapore 903031 (SG).

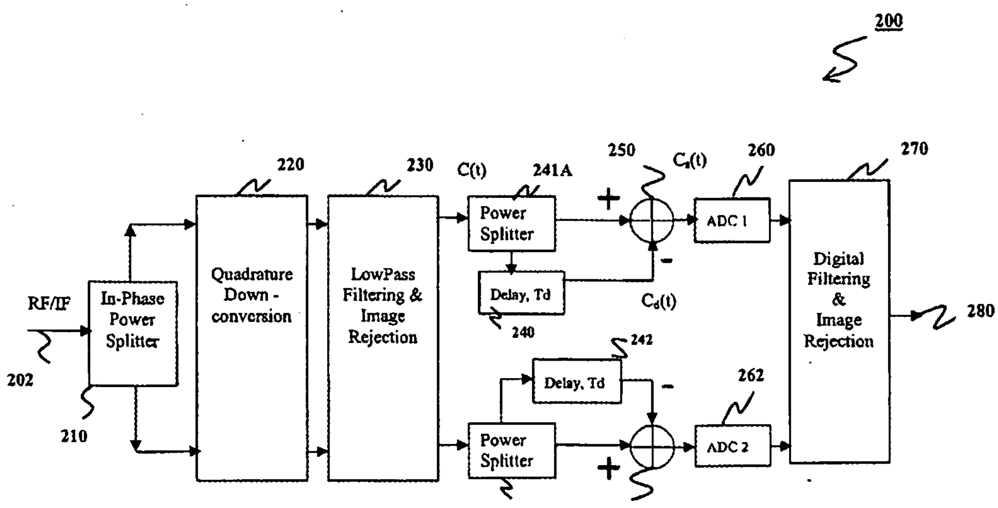
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) Title: HIGH DYNAMIC RANGE RECEIVER



(57) Abstract: A multimode receiver/down converter architecture for use with narrow channel bandwidth and channel bandwidth system signals is described. Interfering signals for a selected narrowband channel are attenuated using a method that reduces the dynamic range of the signal for further processing. The proposed method can be used with a receiver architecture, such as Direct-Conversion, low IF, Super heterodyne, and the like. The downconverted signal is split into two paths. One signal path is delayed and subtracted from the signal from the other path. By controlling the delay value,the interference signals at a given offset are attenuated. Based on the chosen architecture, the desired signal is placed so that the signal undergoes minimal distortion.

WO 03/055086 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

HIGH DYNAMIC RANGE RECEIVER

Field of the Invention

The present invention relates to signal processing systems and more particularly to improved techniques to reduce interference in radio communication systems.

Background

Recently, receivers have been needed that can operate in different communication networks. Existing and proposed communication networks differ in many ways, including operating on different channel bandwidth specifications and different access technologies for multiple users. The differing processing requirements for modem and protocol functions can be realised with programmable components. These multi-system receivers are usually implemented to cater for the wider bandwidth systems hence there is a need for the front end to handle more number of narrow bandwidth channels falling within the wide channel bandwidth of the wideband system. This could be avoided if programmable bandwidth filters are used to do signal channellization in the front end. But programmable bandwidth filters are hard to realize and using multiple filters catering to different bandwidths will make the system bulk and lossy.

Fig. 1 illustrates a simple receiver architecture 100 for these kind of receivers. The receiver architecture 100 includes an antenna 110, a radio frequency (RF) processing and down conversion circuit 110, an analogue-to-digital conversion (ADC) circuit 120, and a baseband processing and data demodulation circuit 130, which are sequentially connected in the foregoing order. Such a receiver architecture 100 requires a signal to be digitised, before different processing can be applied as per modem standards. With different channel bandwidths, the RF processing circuit 110 must be able to handle high dynamic range signals, since multiple channels of a narrow bandwidth system can fit into one channel's bandwidth of a higher bandwidth system. To meet the blocking signal requirements of narrow bandwidth systems that fall within a single wider channel bandwidth, the receiver architecture 100 requires a baseband/intermediate frequency (IF) filter with a bandwidth that can be programmed, or different filters with different bandwidths switched one at a time. This can also be solved by precision filtering in the digital domain, which will require high dynamic range digitizers 120 or much higher oversampling ratios to digitize the required signal along with the blocking signals.

The requirement on ADCs or A/Ds 120 can be reduced by considering the blocking signals as noise overlapping with the required information signal and cancelling the noise out in one of the ways mentioned below. This noise signal can be cancelled out by generating a replica of the blocking signals using prediction techniques and a delayed version of the noise mixed incoming signal and adding in an out-of-phase signal with the incoming signal, as described in U.S. Patent No. 5,903,819 issued to Romesburg on 11 May 1999. Disadvantageously, this type of scheme requires many components to implement and greater processing power to predict the noise signal at IF frequencies. The validity of the replica sample values depends on how fast the noise estimator works and the accuracy of the estimator.

In some schemes as described in U.S. Patent Nos. 3,938,153 issued to Lewis et al. on 10 February 1976 and 3,938,154 issued to Lewis on 10 February 1976, the interfering blocking signals can be isolated using several filters with different bandwidths and/or downconversion using multiple local oscillators and subtracting from the noise mixed downconverted signal. The drawback of this type of scheme is having a number of local oscillators (LOs), mixers, bandpass filters, and subtractors.

Few implementations for the cancellation of blocking signals have multiple antennas and perform some kind of beam steering to attenuate the interfering signals. Other implementations include demodulating the interfering signal and utilising the demodulation information to neutralise the effects of blocking signals. Examples of the foregoing are described in: U.S. Patent Nos. 4,191,926 issued to Pontano et al. on 4 March 1980; 4,222,051 issued to Kretschmer, Jr. et al. on 9 September 1980; 4,736,455 issued to Matsue et al. on 5 April 1988; and 4,384,366 issued to Kaitsuka on 17 May 1983. Any leakage from the transmitter side of a transceiver is cancelled out by extracting a sample of the interfering signal from a coupled signal path of the transmitter and cancelling it out from the incoming received signal after suitable phase detection and adjustments, as described in U.S. Patent No. 4,660,042 issued to Ekstrom on 21 April 1987.

Alternatively as reported in U.S. Patent No. 6,169,912 issued to Zuckerman on 2 January 2001, the interfering transmit band signal is extracted from the receive signal

itself and used to cancel the interference from the received signal. This type of processing requires some kind of filtering to extract a transmit band signal and is not suitable for suppressing blocking signals that are present in the receive frequency band itself.

The effects of blocking signals on actual information data can be cancelled out in the baseband after data demodulation, as described in U.S. Patent No. 4,412,341 issued to Geisho et al. on 25 October 1983.

Interference can also be cancelled after elaborately classifying the interference and then mitigating the interference's effects through targeted interference cancellation, as described in U.S. Patent No. 6,131,013 issued to Bergstrom et al. on 10 October 2000. Though few of these systems are robust, these systems are much easier, or only possible, to implement in the digital domain. This requires high dynamic range ADCs to digitize the signals along with the blocking signals before such processing can be done.

U.S. Patent No. 3,963,990 issued to Di Fonzo on 15 June 1976 describes cross coupling of signals from two different channels in frequency reuse systems to reduce the interference. However, cross coupling is mainly for interference from channels operating in same frequency but channelized in different polarization angles, and basically not for interference from different frequencies.

U.S. Patent No. 6,211,671 issued to Shattil on 3 April 2001 interference cancellation schemes for electromagnetic shielding of electromagnetic pickups, other types of electronic equipment, and specific regions of space. This kind of scheme is not suitable for cancelling out blocking signals, as this scheme relies on phase changes in the pickups at different regions in a receiver to effectively cancel out the interference.

Apart from all the cancellation schemes of the incoming blocking signals, this problem may be solved by "near perfect" digital filtering. Several of the foregoing documents have reported improving the dynamic range of the ADCs, so that these signals can be digitized on whole and the required filtering performed to satisfy the blocking tests. However, all of these schemes are disadvantageously complex and consume more power, which are major drawbacks for implementing such schemes in handset kind of

applications. Thus, a need clearly exists for an improved technique to reduce interference in receiver architectures of radio communication systems.

Summary

In accordance with a first aspect of the invention, there is provided a receiver downconversion architecture for attenuating in an input radiofrequency (RF) signal interfering/blocking signals at offset frequencies from a desired signal. The receiver architecture comprises a delay element having a delay that is dependent on an offset frequency of an interfering signal, and an adder for summing the delayed and instantaneous versions of the input signal.

In accordance with a second aspect of the invention, there is provided a method for, in a receiver downconversion architecture, attenuating in an input radiofrequency (RF) signal interfering/blocking signals at offset frequencies from a desired signal. The method comprising the steps of delaying the input signal dependent on an offset frequency of an interfering signal, and adding delayed and instantaneous versions of the input signal to cancel the interfering/blocking signals.

Brief Description of the Drawings

A small number of embodiments are described hereinafter with reference to the drawings, in which:

Fig. 1 is a block diagram illustrating a conventional, general receiver architecture;

Fig. 2 is a block diagram illustrating a receiver architecture in accordance with an embodiment of the invention for direct conversion with an image reject mixer for very low IF requiring two ADCs;

Fig. 3A is a spectral graph illustrating the spectrum of an incoming RF signal with a desired signal at frequency RF and blocking/interfering signals at frequencies RF $\pm \Delta f$, RF $\pm 2\Delta f$, and so on;

Fig. 3B is a spectral graph illustrating the spectrum of a downconverted signal with the desired signal at ΔF, its image at Δf at a higher signal level, and blocking/interfering signals at 0, $2\Delta f$, $3\Delta f$, and so on;

Fig. 4A is a block diagram illustrating a receiver architecture in accordance with a further embodiment of the invention, which is implemented at IF frequencies for a super-heterodyne receiver architecture;

Fig. 4B is a spectral graph illustrating the spectrum of the downconverted IF signal with the desired signal at IF and blocking/interfering signals at IF ± Δf, IF ± 2Δf, and so on;

Fig. 5 is a spectral graph illustrating phase variation against frequency (through the T_d delay);

Fig. 6A is a block diagram illustrating a receiver architecture in accordance with another embodiment of the invention for direct conversion with an image reject mixer for very low IF requiring two ADCs;

Fig. 6B is a block diagram illustrating another receiver architecture in accordance with a further embodiment of the invention, similar to that of Fig. 6A, requiring 3 ADCs instead of two;

Fig. 3A is a spectral graph of the spectrum of an RF/IF signal at point "*a*" of Fig. 6A, with the spectrum containing the required signal at RF and blocking/interfering signals at RF ± Δf, RF ± 2Δf, and so on;

Fig. 7A is a spectral graph of the downconverted RF/IF signal spectrum at point "*b*" in Fig. 6A;

Fig. 7B is a spectral graph of the downconverted RF/IF spectrum after filtering at point "c" in Fig. 6A;

Fig. 7C is the spectral graph of the downconverted, filtered signal after phase shifting and combining with the in-phase downconverted signal at point "d" in Fig. 6A;

Fig. 7D is a spectral graph of the image suppressed signal that is delayed and combined with the feed-through signal at point "e" in Fig. 6A;

Fig. 7E is a spectral graph of the interference and image cancelled signal that is digitised and further filtered and baseband processed; and

Fig. 8 is a schematic diagram of a switched-capacitor delay line and summer configuration in accordance with a further embodiment of the invention.

Detailed Description

A multi-mode receiver/downconverter architecture for use with narrow channel bandwidth and wide channel bandwidth system signals is described. In this architecture, interfering signals for a selected narrowband channel are attenuated using a technique that

reduces the dynamic range of the signal for further processing. The technique can be used with receiver architectures, such as direct-conversion, low IF, super heterodyne, and the like. In this technique, the downconverted signal is split into two paths. One signal path is delayed and subtracted from the signal from the other path. By controlling the delay value, the interference signals at a given offset are attenuated. Based on the chosen architecture, the desired signal is placed so that the desired signal undergoes minimum distortion.

The embodiments of the invention attenuate the interfering signals for narrowband systems, which otherwise pass through a wider bandwidth baseband/IF filter catering for the wider bandwidth signals sufficiently enough to reduce the dynamic range requirements of ADCs in the receive chain.

Fig. 2 is a block diagram showing a direct-conversion type of receiver architecture 200. An RF/IF signal 202 is input to an in-phase power splitter 210. Two signals are provided to a quadrature down-conversion circuit 220, which provides two outputs to low pass filtering and image rejection circuit 230. A signal C(t) output by the circuit 230 is split by the power splitter 241A and provided to a summer 250 and a delay module 240, which has a delay T_d. A delayed signal $C_d(t)$ is provided to a negative input of the summer 250. The summer 250 outputs the resulting signal $C_s(t)$ to a first ADC module 260. The output of this ADC 260 is provided to digital filtering and image rejection circuit 270. A completely equivalent circuit comprising delay 242, summer 252 and ADC 262 is coupled between the other output of the low pass filtering and image rejection circuit 230 and the other input of digital filtering and image rejection circuit 270. An output signal 280 is produced from circuit 270. Thus, the downconverted I & Q signals are split into two paths each using power splitters 241A & 241B. One path in each branch is delayed 240, 242 and fed forward and subtracted 250, 252 from the undelayed path as shown in Fig. 2.

The narrowband signal is quadrature downconverted using an image reject mixer such that desired signal is positioned at a frequency ΔF and it falls at the upper edge of the much wider baseband filter 310 as shown in Figs. 3A and 3B. In particular, Fig. 3A illustrates the spectrum of the incoming RF signal, and Fig. 3B shows the downconverted signal with the desired signal, its image, and blocking/interfering signals. The blocking

signals on the lower side of the signals fall close to the DC value. The image signal is superimposed on the desired signal. The upper side blocking signals at $2\Delta F$, $3\Delta F$, and so on are cut-off by the filter bandwidth roll off 310, as shown in Fig. 3B. The attenuation characteristic for this embodiment is shown with a dotted line in Fig. 3B.

A simple way to calculate the amount of delay to be introduced for addition or subtraction of the signals is described hereinafter. Assuming that the information signal is a phase-shift key (PSK) signal S(t) and the interfering/blocking signal is also a PSK signal X(t), the signals can be written

$$S(t) = A\cos[\omega_c t + \phi_c(t)],$$
$$X(t) = B\cos[\omega_i t + \phi_i(t)],$$

where: $\phi_c(t)$ and $\phi_i(t)$ are the instantaneous phases;
$\omega_c = 2\pi f_c$; f_c is the required channel carrier frequency;
$\omega_i = 2\pi f_i$; f_i is the interfering channel carrier frequency;
$f_i = f_c + \Delta f$; and Δf is the offset of the interfering signal from the desired signal frequency.

In Fig. 2,

$$C(t) = S(t) + X(t), \text{ and}$$
$$C_d(t) = C(t-T_d).$$

Assuming that the delay T_d is small enough, the phase $\phi_c(t- T_d)$ and $\phi_i(t- T_d)$ can be approximated to $\phi_c(t)$ and $\phi_i(t)$.

In $C_s(t) = C(t) - C_d(t)$, the information signal adds up and the interfering signal is cancelled out, if:

$$T_d = 1/(2^*\Delta f); \text{ and}$$
$$f_c = a * \Delta f ; a = 1, 3, 5, 7, \ldots \text{ ('a' is an odd integer).}$$

This relationship is valid for direct downconversion, low IF downconversion and the conventional Super heterodyne architecture using higher IF. Importantly the relationship between the carrier frequency and the offset frequency of the interfering signal requiring maximum cancellation is that the carrier frequency should be an odd multiple of the offset frequency of the interference. So that the required signal undergoes 180° phase shift and the interfering signal is phase shifted by zero or multiples 360° phase shift. When the delayed and feed forward paths are subtracted the 180° phase shifted carrier adds up and the other interfering signal cancels out. The scheme can be modified to use a summer instead of a subtractor, in which case the interfering signal will be phase shifted by 180° and the required signal by zero or multiples of 360°.

From the above analysis, by controlling the delay (equal to $1/(2*\Delta f)$) in the feed forward path, the unwanted blocking signals can be cancelled out or attenuated, and the required signals can be added up. The amount of cancellation depends on the amount of phase shift the fixed delay line imparts to the signals and how far the amplitudes of the delayed and instantaneous signals are matched. The amount of cancellation can be quantitatively calculated based on the amplitude and phase error in the two paths. This is also true for instantaneous frequency components in the signal spectrum. For the required signal not to be distorted, the delay has to be sufficiently less than the inverse of the bandwidth of the data modulated on to the required carrier. The delay can be implemented as a fixed delay element for a particular offset frequency to be cancelled or can be made a programmable delay that can be varied to cancel signals at a particular offset. Fig. 5 shows the phase variations of the signals with different frequencies, when delayed by T_d.

Fig. 4 shows another embodiment of the invention implemented at IF frequency for a Super-Heterodyne receiver architecture. The receiver architecture 400 of Fig. 4A includes an RF processing and downconversion circuit 410, an IF band pass filter 420, a power splitter 422, a delay module 430, an ADC 450, and a digital filtering, downconversion, baseband processing, and data demodulation circuit 460. The output of the circuit 410 is coupled to the input of the bandpass filter 420. The output of the bandpass filter 420 is split using power splitter 422 and provided to a positive input of summer 440 and the delay circuit 430, which provides the delay T_d. The output of the delay circuit 430 is provided to a negative input of the summer 440. The output of the

summer 440 is provided to the ADC 450. In turn, the output of the ADC 450 is provided to the circuit 460.

In this case, the desired signal is downconverted to the IF frequency and the interfering signals at both sides of the IF frequency are attenuated. Depending on the amount of phase shift the delay introduces to the signals, the signals are cancelled or added up.

In the case of the super-heterodyne downconversion architecture, the splitter, delay and subtraction technique (430, 440) is implemented after the IF Bandpass filter (420), which cuts off the far off blocking signals. Depending on the offset frequency of the interfering signal, the fixed/variable delay value T_d is calculated. The IF frequency also has to be fixed in such a way that this frequency satisfies the above mentioned conditions.

Fig. 3A illustrates the spectrum of the incoming RF signal received at the input of the circuit 410, with the desired signal at frequency RF and blocking/interfering signals at RF $\pm$ Δf, RF $\pm$ 2Δf, and so on. Fig. 4B illustrates the spectrum of the downconverted IF signal with the desired signal at frequency IF and blocking/interfering signals at IF $\pm$ 1Δf, IF $\pm$ 2Δf, and so on. Fig. 4B illustrates the IF bandpass filter characteristic 470 provided by bandpass filter 420 in Fig. 4A. Also shown with dotted lines are the attenuation characteristics 480 provided by this technique. The interference/blocking signals within the baseband filter's passband are attenuated by the attenuation characteristic 480. The interference/blocking signals outside the passband are attenuated by the BPF characteristic 470.

In the case of quadrature direct downconversion scheme, there is a problem of the image signal, which overlaps with the required signal after downconversion. If the offset frequency is based on the blocking signal, the image frequency signal may be a blocking signal of the narrowband system and be of much higher magnitude than the required signal level. This image frequency has to be removed before any further processing and can be removed by using a image reject mixer architecture.

Fig. 6A is a block diagram of a receiver architecture utilising direct conversion with image reject for very low IF utilising two ADCs. The RF/IF signal is provided at point "a" as input to the in-phase power splitter 610. The splitter 610 provides respective outputs to mixers 612 and 614. A local oscillator (LO) provides another input directly to the mixer 612, and a 90° phase delayed signal, produced by the delay element 616, to the other mixer 614. The output of mixer 612 is labelled point "b" and provided to low pass filter 620. Likewise, the output of mixer 614 is provided to low pass filter 622. The output of low pass filter 620 and splitter 621A is labelled point "c" and provided to the summer 630 and 90° phase shifter 624. Similarly, the output of low pass filter 622 is split using splitter 621B and provided to a positive input of summer 632 and a -90° phase shifter 626. The outputs of phase shifters 624 and 626 are provided to respective inputs of summers 630 and 632. The output of the summer 630 is split using splitter 631A and labelled point "d" and provided as input to summer 650 and delay element 640a. The output of delay element 640a, which provides delay T_d, is provided to the negative input of a summer 650. Likewise, the output of summer 632 is split using splitter 631B and provided as input to summer 652 and a delay element 640b. The output of delay element 640b is provided to a negative input of the summer 652. The output of the summer 650 is labelled point "e" and provided to an ADC 660. Likewise, the output of the summer 652 is provided to an ADC 662. The outputs of ADCs 660 and 662 are provided to digital filtering and image rejection module 670. The output of module 670 is labelled point "f".

Fig. 6B is a block diagram illustrating a further embodiment of the invention involving direct conversion with image reject for very low IF requiring three ADCs. The configuration of this circuit is the same as that of Fig. 6A in relation to elements 610, 612, 614, 616, 620, 622 and 623. The output of the power splitter 623 is provided as input to –90° phase shifter 626, a positive input of a summer 632, and another positive input of the summer 632 is fed with quadrature downconverted signal to cancel the image frequency and extract the required signal. The extracted required signal is provided to the delay element 640B which provides delay T_d. When the delayed and the feed forward paths are subtracted 680, the interfering signal cancels out depending on the delay T_d. This signal is digitised by ADC 690 and provided to module Digital Filtering and Image Rejection module 670. The outputs of low pass filters 620 and power splitter 623 are passed directly to the ADCs 660 & 662, which provide outputs to the digital filtering and image rejection

module 670. In the module 670, the required signal is filtered and Image signal is further cancelled/attenuated by standard filtering and image cancellation techniques.

Figs. 7A – 7E show signal spectrum at different stages of the circuit Fig. 6A

Fig. 7A illustrates the downconverted RF/IF signal spectrum at point "b" of Fig. 6A. The spectrum is shifted to the baseband with the required signal at Δf and the blocking/interfering signals at 0, 2Δf, 3Δf, and so on. In the spectral graph, the image signal is seen overlapping the required signal at frequency Δf.

Fig. 7B is a spectral graph illustrating the spectrum at point "c" of Fig. 6A. The low pass filter characteristic 710 of low pass filter 620 is shown. The downconverted RF/IF signal spectrum is filtered for sum components and other interferences. The spectrum has the blocking/interfering signals at 2Δf, 3Δf, and so on, attenuated by the low pass filter characteristic 710. The blocking/interfering signals at frequency 0 and the image signal overlapping on the desired signal at frequency Δf are still significant.

Fig. 7C is a spectral graph of the signal spectrum at point "d" of Fig. 6A. The downconverted, filtered signal is 90° phase shifted and combined with an in-phase downconverted signal. The spectrum has the image signal (overlapping on the required signal at frequency Δf) significantly attenuated.

Fig. 7D is a spectral graph illustrating the spectrum at point "e" of Fig. 6A. The image suppressed signal is delayed and combined with the feed-through signal at ΔF, which attenuates the interfering signal at frequency 0. Fig. 7D illustrates the proposed attenuation characteristic 720. The amount of attenuation depends on the phase shift provided by the delay element 640A. The spectrum shown has the image signal (overlapping on the required signal at frequency Δf) and the interfering signal at frequency 0 attenuated.

The module 670 provides at its output the signal at point F of Fig. 6A. Fig. 7E is a spectral graph illustrating the interference and image cancelled signal that is digitised and further filtered and baseband processed. This is done to attenuate the interfering signal at frequency 0 and the image signal (overlapping on the required signal at

frequency Δf). After this, the required signal at frequency Δf can be further digitally downconverted for further processing.

The use of image reject mixer architecture may not attenuate the image frequency completely and depends on the 90 degree hybrid used to combine the quadrature down converted signal and the signal path lengths after downconversion. As the proposed technique may be used for narrowband signals, the 90 degree hybrid meeting the requirements in the narrow band of interest is sufficient. The attenuation of the blocking/interfering signals leads to the reduction in the dynamic range requirements of the ADC for digitisation and subsequent processing of the multi-mode signals.

The delay T_d can be implemented in many ways, examples of which are listed below.

One method uses a simple length of cable or a transmission line having an electrical length that is adjusted so that the cable gives the required delay as calculated above for the required offset frequency. The length of cable can be numerically estimated based on the velocity of electromagnetic (EM) waves in the material in which cable is realised.

Another method integrates the delay into the A/D conversion process. Once the signal is sampled and held, the signal can be split into two paths. One path can be delayed using switched capacitor circuits and combined with the main path samples before quantization. By this way, the limitations on the sample and hold amplifier remain, but the quantizer sees attenuated levels of the blocking signals. The quantizations levels in the quantizer can be set to maximise the dynamic range with reduced number of bits and suitable gain amplifiers can be used to maximise the use of the dynamic range of the quantizer. Figure 8 shows a typical example of an implementation using switched capacitor techniques. The switched capacitor delay line when implemented can be made to give a different values of delay depending on the clock frequencies used to turn ON and OFF the switches and the number of unit delay stages used. A more detailed description on the working of the circuit is given in Eriksson, S., "Realisation of Switched capacitor delay lines and Hilbert transformers", Electronics Letters, July 1991, Vol 27, No 14., pp 1262-1263.

Thus, a multimode receiver/downconverter architecture has been described. While only a small number of embodiments have been described, it will be apparetn to those skilled in the art that, in the light of this disclosure, modifications and variations can be made without departing from the scope and spirit of the invention.

CLAIMS:

1. A receiver downconversion architecture for attenuating in an input radiofrequency (RF) signal interfering/blocking signals at offset frequencies from a desired signal, said receiver architecture comprising:

a delay element having a delay that is dependent on an offset frequency of an interfering signal; and

an adder for summing/subtracting delayed and instantaneous versions of said input signal based on the phase relationship between the signals.

2. The receiver downconversion architecture as claimed in claim 1, wherein said cancellation results in undesired signals in said input signal being attenuated such that dynamic range requirements for analog-to-digital conversion are reduced.

3. The receiver downconversion architecture as claimed in claim 1, further comprising means for modifying a direct-conversion architecture to offset said desired signal by an offset frequency at least approximate to a frequency offset of at least one critical interfering signal.

4. The receiver downconversion architecture as claimed in claim 1, wherein said delay is equal to $T_d = 1/(2*\Delta f)$, where Δf is equal to said frequency offset of said at least one critical interfering signal relative to said desired signal.

5. The receiver downconversion architecture as claimed in claim 1, wherein said delay element is implemented using transmission lines.

6. The receiver downconversion architecture as claimed in claim 1, wherein said delay and said adder are implemented using switched capacitor and operational amplifiers.

7. The receiver downconversion architecture as claimed in claim 1, wherein said delay and said adder are integrated with a frontend of an analog-to-digital converter (ADC).

8. The receiver downconversion architecture as claimed in claim 1, further comprising means for converting said desired signal to an intermediate frequency (IF) equal to an odd multiple of $\Delta f = 1/(2^* T_d)$, where T_d is said delay of said delay element.

9. The receiver downconversion architecture as claimed in claim 1, wherein said delay element is programmable.

10. The receiver downconversion architecture as claimed in claim 1, further including a Low Frequency intermediate frequency (IF)/Zero IF architecture.

11. The receiver downconversion architecture as claimed in claim 10, further comprising a mixer, where said desired signal is consequently positioned at an upper end of a low pass spectrum.

12. The receiver downconversion architecture as claimed in claim 1, comprising a Super Heterodyne architecture with an intermediate frequency (IF) equal to an odd multiple of a frequency offset with interference.

13. A method for, in a receiver downconversion architecture, attenuating in an input radiofrequency (RF) signal interfering/blocking signals at offset frequencies from a desired signal, said method comprising the steps of:

delaying said input signal dependent on an offset frequency of an interfering signal; and

adding delayed and instantaneous versions of said input signal to cancel said interfering/blocking signals.

14. The method as claimed in claim 13, wherein said cancellation results in undesired signals in said input signal being attenuated such that dynamic range requirements for analog-to-digital conversion are reduced.

15. The method as claimed in claim 13, further including the step of modifying operation of a direct-conversion architecture to offset said desired signal by an

offset frequency at least approximate to a frequency offset of at least one critical interfering signal.

16. The method as claimed in claim 13, wherein a delay generated by said delaying step is equal to $T_d = 1/(2*\Delta f)$, where Δf is equal to said frequency offset of said at least one critical interfering signal relative to said desired signal.

17. The method as claimed in claim 13, wherein said delaying step is implemented using transmission lines.

18. The method as claimed in claim 13, wherein said delaying and said adding steps are implemented using switched capacitor and operational amplifiers.

19. The method as claimed in claim 13, wherein said delaying and said adding are implemented with circuitry integrated with a frontend of an analog-to-digital converter (ADC).

20. The method as claimed in claim 13, further including the step of converting said desired signal to an intermediate frequency (IF) equal to an odd multiple of $\Delta f = 1/(2* T_d)$, where T_d is said delay of said delay element.

21. The method as claimed in claim 13, wherein a delay generated by said delaying step is programmable.

22. The method as claimed in claim 13, wherein said receiver downconversion architecture includes a Low Frequency intermediate frequency (IF)/Zero IF architecture.

23. The method as claimed in claim 22, further including the step of mixing so that said desired signal is consequently positioned at an upper end of a low pass spectrum.

24. The method as claimed in claim 13, wherein said receiver downconversion architecture comprises a Super Heterodyne architecture with an intermediate frequency (IF) equal to an odd multiple of a frequency offset with interference.

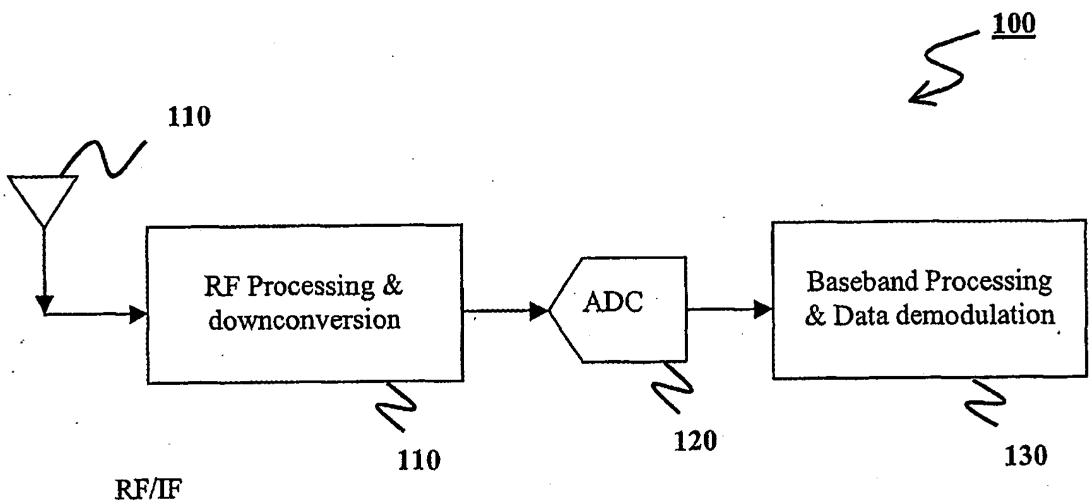

100
110
RF Processing & downconversion
ADC
Baseband Processing & Data demodulation
110
120
130
RF/IF

FIG. 1

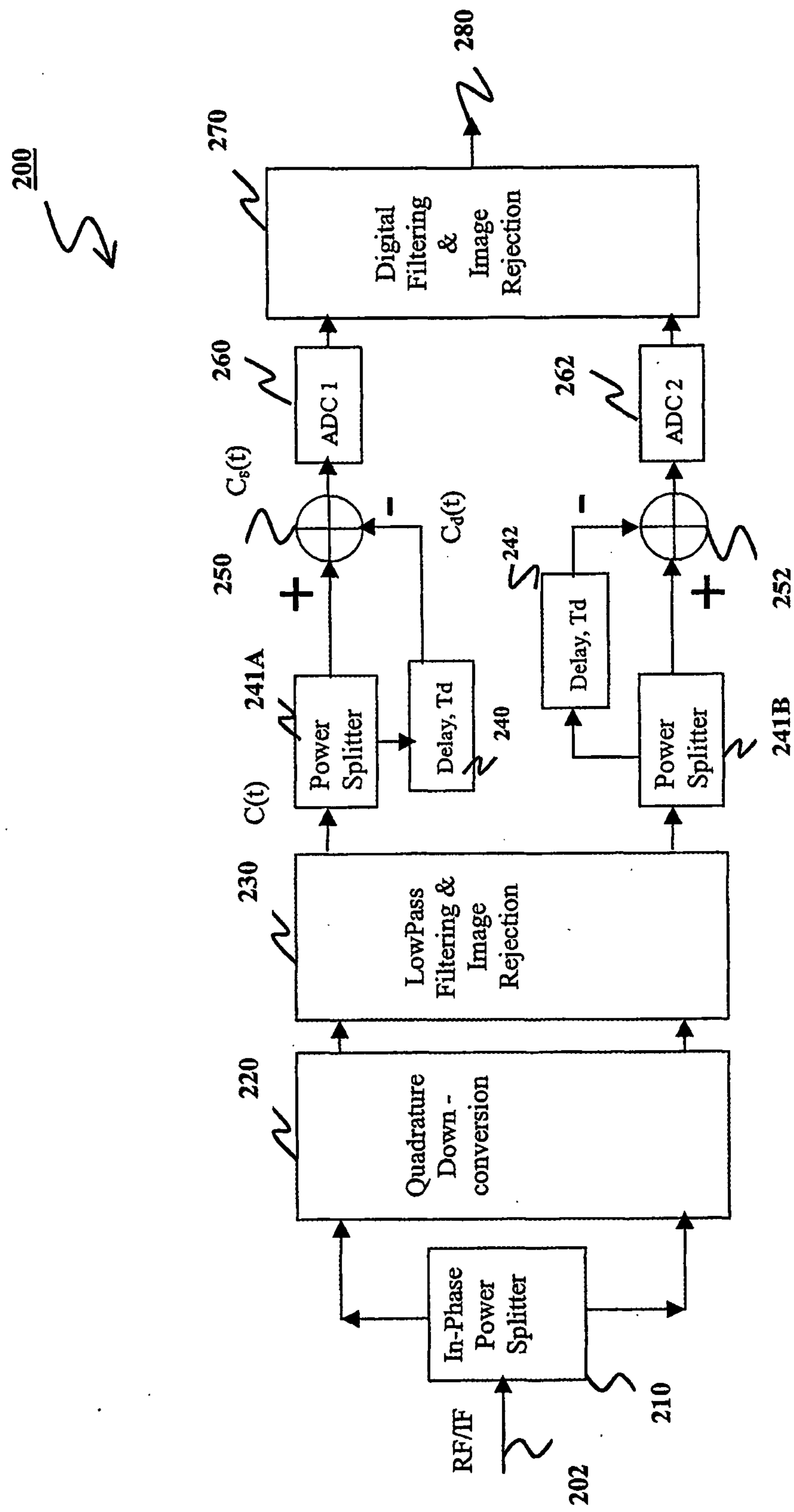

200
270
280
Digital Filtering & Image Rejection
260
ADC 1
262
ADC 2
$C_s(t)$
-
$C_d(t)$
250
+
242
Delay, Td
-
+
252
241A
Power Splitter
Delay, Td
240
Power Splitter
241B
C(t)
230
LowPass Filtering & Image Rejection
220
Quadrature Down - conversion
In-Phase Power Splitter
RF/IF
202
210

FIG. 2

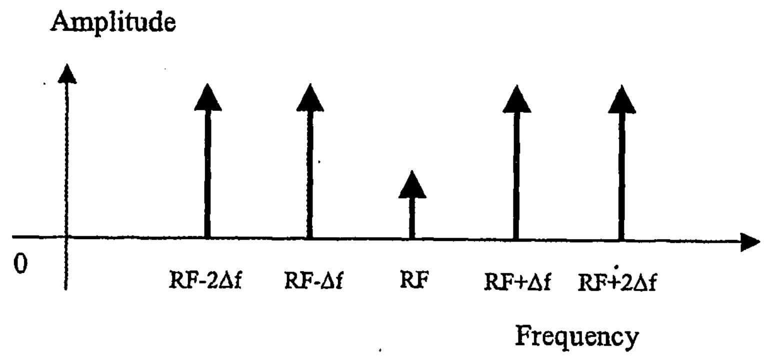

Amplitude
0
RF-2Δf
RF-Δf
RF
RF+Δf
RF+2Δf
Frequency

FIG. 3A

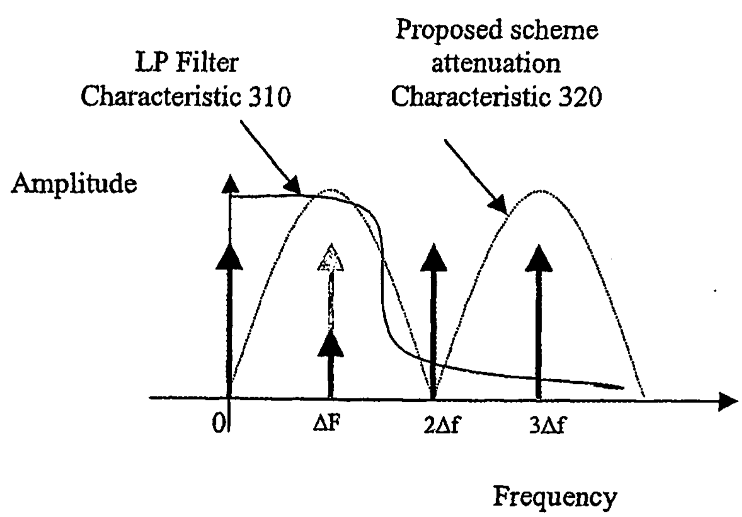

Proposed scheme
attenuation
Characteristic 320
LP Filter
Characteristic 310
Amplitude
0
ΔF
2Δf
3Δf
Frequency

FIG. 3B

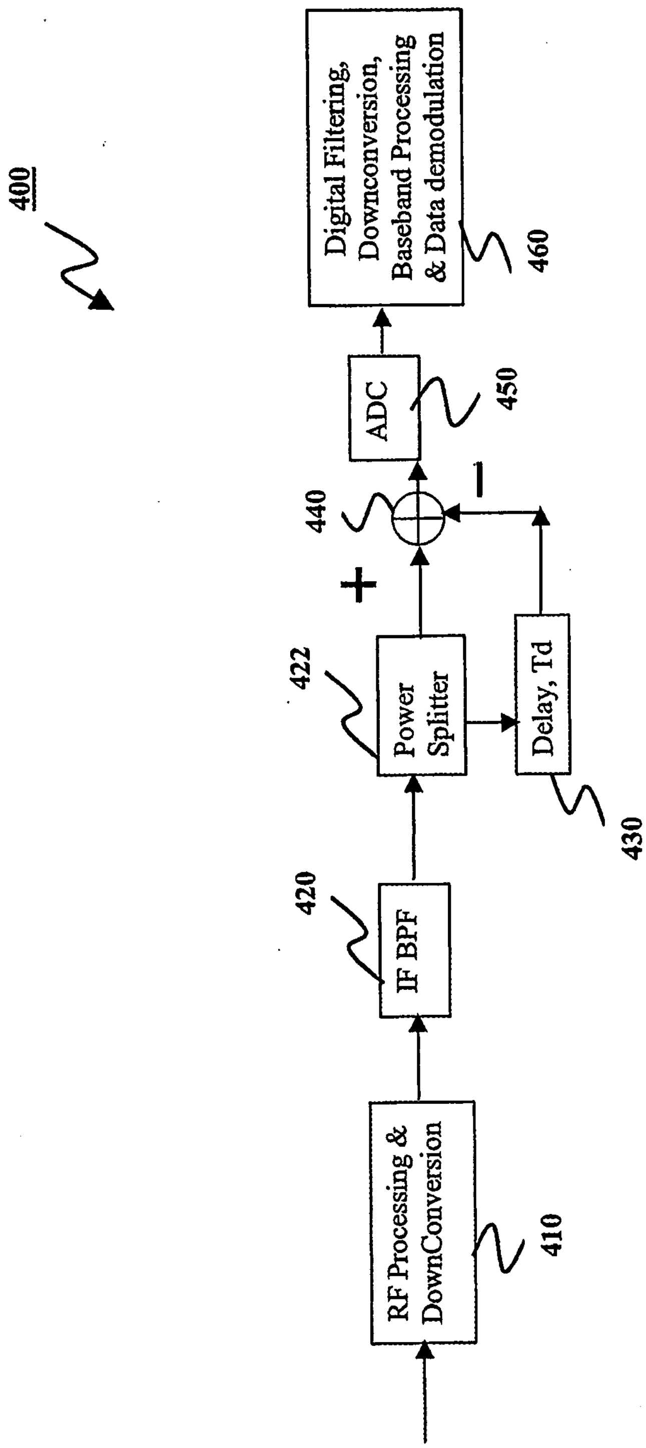

400
Digital Filtering, Downconversion, Baseband Processing & Data demodulation
460
ADC
450
440
+
-
Power Splitter
422
Delay, Td
430
IF BPF
420
RF Processing & DownConversion
410

FIG. 4A

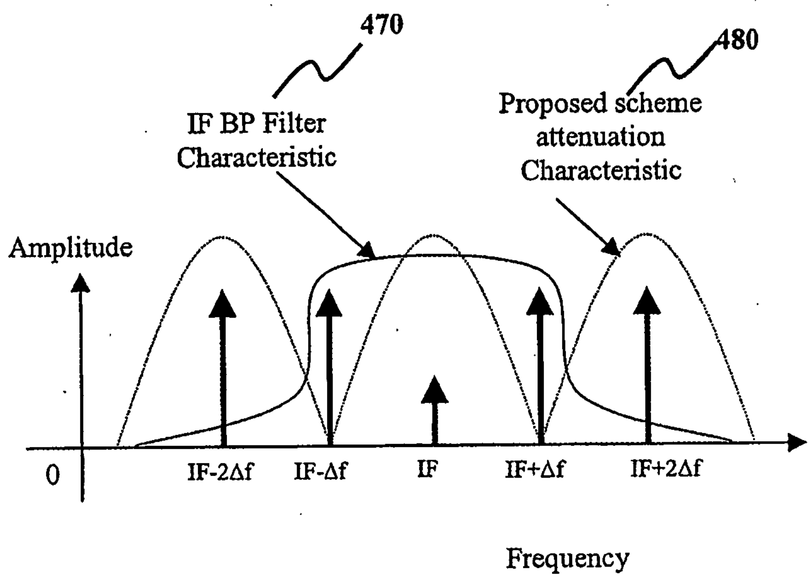

470
480
IF BP Filter
Characteristic
Proposed scheme
attenuation
Characteristic
Amplitude
0
IF-2Δf
IF-Δf
IF
IF+Δf
IF+2Δf
Frequency

FIG. 4B

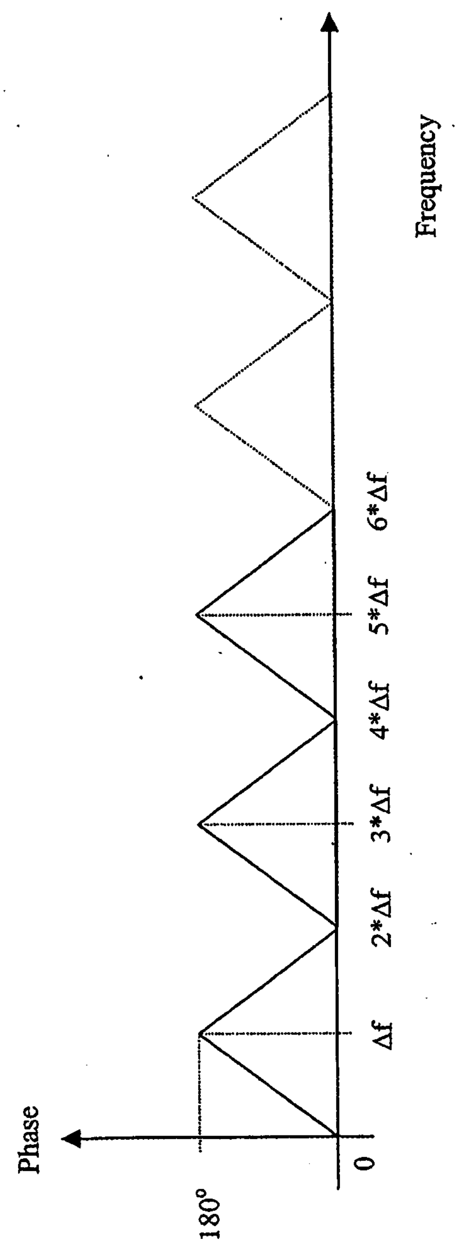


FIG. 5

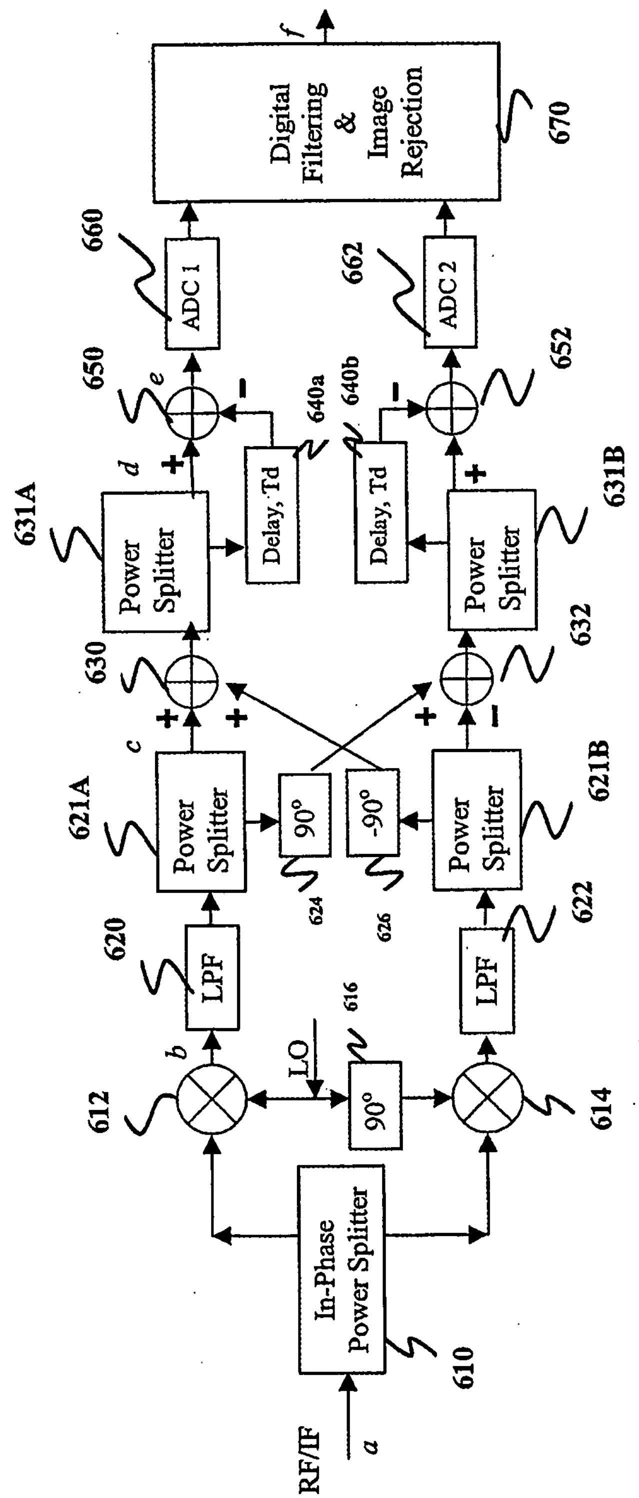

RF/IF
a
In-Phase Power Splitter
610
612
614
LO
616
90°
b
LPF
620
LPF
622
Power Splitter
621A
Power Splitter
621B
c
90°
-90°
624
626
630
632
Power Splitter
631A
Power Splitter
631B
d
Delay, Td
640a
Delay, Td
640b
e
650
652
ADC 1
660
ADC 2
662
Digital Filtering & Image Rejection
670
f

FIG. 6A

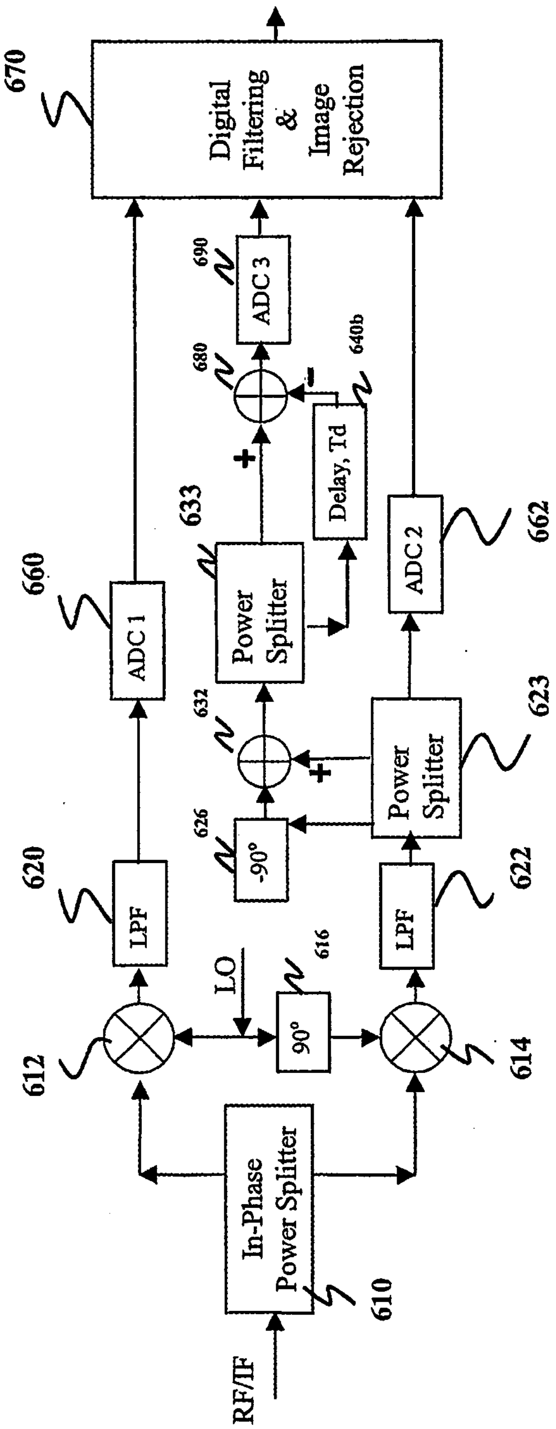

670
Digital
Filtering
&
Image
Rejection
660
ADC 1
690
ADC 3
680
640b
Delay, Td
633
Power
Splitter
662
ADC 2
632
623
Power
Splitter
626
-90°
620
LPF
622
LPF
LO
616
90°
612
614
In-Phase
Power Splitter
610
RF/IF

FIG. 6B

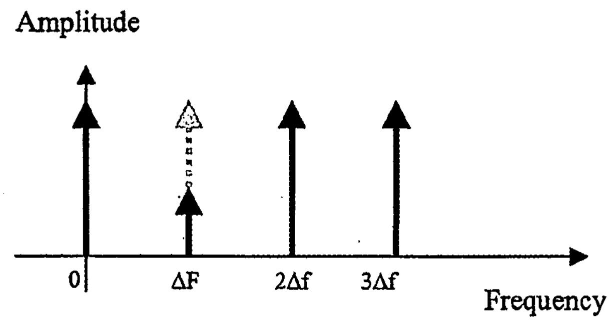


FIG. 7A

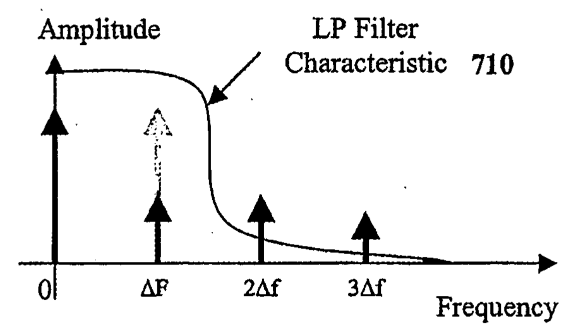


FIG. 7B

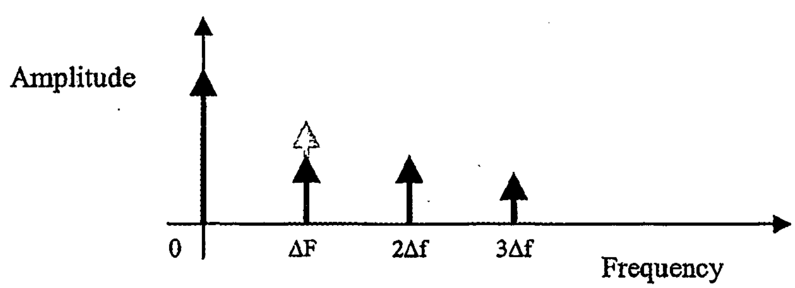


FIG. 7C

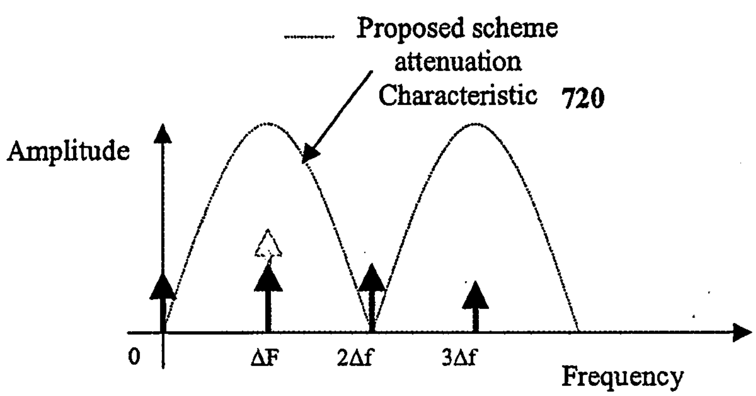

Proposed scheme
attenuation
Characteristic 720
Amplitude
0
ΔF
2Δf
3Δf
Frequency

FIG. 7D

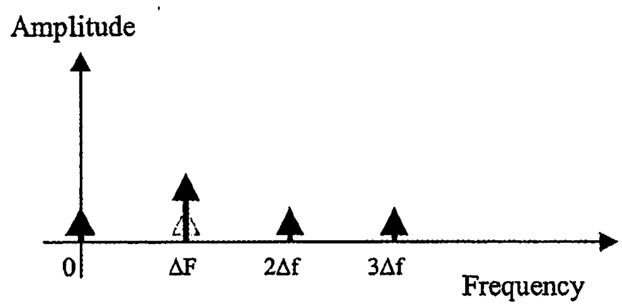

Amplitude
0
ΔF
2Δf
3Δf
Frequency

FIG. 7E

800

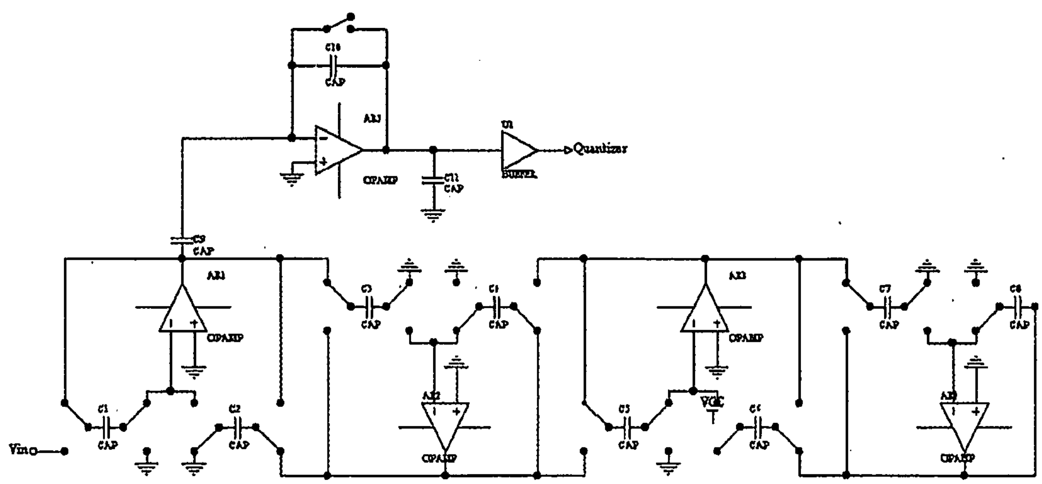


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG 01/00256

CLASSIFICATION OF SUBJECT MATTER

IPC[7]: H04B 1/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC[7]: H04B 1/00, 1/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4991165 A (W.M. CRONYN) 5 February 1991 (05.02.91) *the whole document.*	1-24
A	US 4736455 A (M. MATSUE & T. MURASE) 5 April 1988 (05.04.88) *the whole document.*	1-24

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
„A" document defining the general state of the art which is not considered to be of particular relevance
„E" earlier application or patent but published on or after the international filing date
„L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
„O" document referring to an oral disclosure, use, exhibition or other means
„P" document published prior to the international filing date but later than the priority date claimed
„T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
„X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
„Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
„&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 November 2002 (28.11.2002)	31 January 2003 (31.01.2003)

Name and mailing adress of the ISA/AT	Authorized officer
Austrian Patent Office Kohlmarkt 8-10; A-1014 Vienna Facsimile No. 1/53424/535	ZUGAREK G. Telephone No. 1/53424/383

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/SG 01/00256

Patent document cited in search report			Publication date	Patent family member(s)			Publication date
US	A	4736455	05-04-1988	CA	A1	1257658	18-07-1989
				DE	C0	3685645	16-07-1992
				DE	T2	3685645	21-01-1993
				EP	A2	228786	15-07-1987
				EP	A3	228786	21-09-1988
				EP	B1	228786	10-06-1992
				JP	A2	62147818	01-07-1987
				JP	B4	7061023	28-06-1995
				JP	A2	62219035	28-09-1987
				JP	B4	6105897	21-12-1994
				JP	A2	62219836	28-09-1987
				JP	A2	62233942	14-10-1987
				JP	B4	6105898	21-12-1994
				JP	A2	62233943	14-10-1987
				JP	B4	6105899	21-12-1994
US	A	4991165	05-02-1991			none	

PCT/ISA/210 (patent family annex) (July 1998)